REMARKS

Claims 1-3 are pending. Claim 1 has been amended. Claims 4-6 have been cancelled without prejudice or disclaimer as to Applicant's right to pursue the subject matter of these claims in a continuing application. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Applicant appreciates the courtesies extended to the Applicant's representative during the February 27, 2004 personal interview with the Examiner. During the interview, Applicant's representative discussed that the Gardner reference (U.S. patent No. 6,077,748) did not teach or suggest a second electrode because the conducting path was not a second electrode. The Examiner agreed. Further, Applicant's representative discussed that it would not be obvious to a person skilled in the art to divide the single electrode 70 (Gardner) or 107 (Mitani U.S. Patent No. 6,018,185) to form a first and second electrode. The Examiner continued to hold his position that it would be obvious. Lastly, Applicant's representative argued that even if the electrodes were divided, no combination of Gardner and Mitani teach or suggest an oxide layer formed on a side wall of only the first gate electrode, as recited in claim 1. The Examiner agreed. The above arguments are provided below with additional detail in relation to the rejections in the Office Action.

Claim Rejection Under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(e) over Gardner et al. (U.S. Patent No. 6,077,748). Applicant respectfully traverses this rejection

Claim 1 recites, in part, a transistor which includes a gate electrode structure. The gate electrode structure includes a stacked structure of a gate oxide film, a first gate electrode and a second electrode, an oxide layer formed on a side wall of only the first gate electrode, and nitride spacers formed on the oxide layer on the sidewall of the first gate electrode and on a side wall of the device isolation film. In contrast, Gardner merely discloses a conducting path 82 formed in conducting via holes 92 and on polysilicon layer 70. Gardner fails to teach a stacked structure including a first and second gate electrode as recited in claim 1.

The Office Action alleges that the conducting path 82 corresponds to the second electrode recited in claim 1. Applicants respectfully disagree.

The conducting path 82 and the via holes 92, described in Gardner, provide distribution of signals within the integrated circuit (column 5, lines 35-40). In fact, Gardner specifically recites that the gate structure includes only 68 and 70 (i.e., the dielectric layer 68 and polysilicon layer 70) (column 4, line 41). Accordingly, Gardner does not teach or suggest

a stacked structure of a gate oxide film, a first gate electrode and a second electrode, as recited in claim 1.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claim Rejection Under 35 U.S.C. § 103

Claims 1-3 were rejected under 35 U.S.C. § 103(a) over Mitani (U.S. patent No. 6,018,185) in view of Gardner. Applicant respectfully traverse this rejection.

Claim 1 recites, in part, a transistor which includes a gate electrode structure. The gate electrode structure includes a stacked structure of a gate oxide film, a first gate electrode and a second electrode, an oxide layer formed on a side wall of only the first gate electrode, and nitride spacers formed on the oxide layer on the sidewall of the first gate electrode and on a side wall of the device isolation film. In contrast, Mitani discloses a single gate electrode on an insulation film. Mitani fails to teach or suggest a first and second gate electrode. The Office Action alleges that the electrode 107 could be formed by forming two sequential layers since separating what was once one layer into many layers involves only routine skill (pages 5 and 6). Applicants respectfully disagree. Mitani does not teach or suggest separating the layer 107 into multiple layer. In fact, Mitani specifically teaches that the electrode 107 is formed by a single phosphorous doped polycrystalline silicon film (column 8, lines 20-21). Gardner does not remedy this deficiency because Gardner merely teaches a single gate electrode as discussed above.

Further, as admitted in the Office Action (page 6), the insulation film 109 is formed on the side wall of the entire gate electrode 107. Therefore, even if Mitani was construed as suggesting that the single layer could be multiple layers, Mitani still fails to teach or suggest an oxide layer formed on a side wall of only the first gate electrode, as recited in claim 1. Additionally, Gardenr does not remedy this deficiency since Gardner merely discloses a single gate electrode. Accordingly, no combination of Mitani and Gardner teach or suggest a first gate electrode and a second electrode, an oxide layer formed on a side wall of only the first gate electrode, as recited in claim 1.

Claims 2 and 3 are believe allowable for at least the reasons presented above with respect to claim 1 by virtue of their dependence upon claim 1. Accordingly, Applicant respectfully traverses this rejection.

Conclusion

In view of the foregoing, the claims are believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Please charge any fees associated with the submission of this paper to Deposit Account Number 03-3975 under Order No. 82124/275428. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

Pillsbury Winthrop LLP

By: Caroline D. Dennison

Caroline D. Dennison
Reg. No.: 34,494
Vishal V. Khatri
Reg. No.: 51,873
Tel. No.: (703) 905-2047
Fax No.: (703) 905-2500

CDD\VVK

Customer Number [00909]